

Appl. No. 10/644,490
Amdt. dated 9/13/05
Reply to Office Action of 6/13/05

PATENT
Docket: 030284

IN THE CLAIMS

Please amend the claims as follows:

1. (Original) An integrated circuit comprising:
a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phases of the reference and feedback signals to determine a phase error between the reference and feedback signals, and provide a PFD output comprised of PFD values, wherein each PFD value is a multi-bit value determined by the phase error and a detector gain; and
a loop filter (LF) operative to receive and filter the PFD output and provide an LF output, wherein the LF output is updated for each PFD value received on the PFD output.
2. (Original) The integrated circuit of claim 1, further comprising:
an oscillator operative to receive the LF output and provide an oscillator signal having a phase determined by the LF output; and
a divider operative to receive the oscillator signal, divide the oscillator signal in frequency by a factor of N, where N is one or greater, and provide the feedback signal.
3. (Original) The integrated circuit of claim 1, wherein the detector gain is adjusted in an acquisition mode and maintained in a tracking mode.
4. (Original) The integrated circuit of claim 1, wherein the detector gain is initialized to a maximum value and thereafter decreased whenever a change in phase error polarity is detected.
5. (Original) The integrated circuit of claim 1, wherein the PFD is further operative to provide a clock signal having a pulse for each PFD value in the PFD output, and wherein the loop filter is operative to update the LF output with the clock signal.
6. (Original) The integrated circuit of claim 5, wherein the pulse in the clock signal for each PFD value is delayed by a particular amount of time relative to a start of the PFD value.

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7. (Original) A device comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phases of the reference and feedback signals to determine a phase error between the reference and feedback signals, and provide a PFD output comprised of PFD values, wherein each PFD value is a multi-bit value determined by the phase error and a detector gain; and

a loop filter (LF) operative to receive and filter the PFD output and provide an LF output, wherein the LF output is updated for each PFD value received on the PFD output.

8. (Original) An apparatus comprising:

means for comparing phases of a reference signal and a feedback signal to determine a phase error between the reference and feedback signals;

means for providing a phase-frequency detector (PFD) output comprised of PFD values, wherein each PFD value is a multi-bit value determined by the phase error and a detector gain;

means for filtering the PFD output to obtain a loop filter (LF) output;

means for providing an oscillator signal having a phase determined by the LF output; and

means for dividing the oscillator signal in frequency by a factor of N to obtain the feedback signal, where N is one or greater.

9. (Currently Amended) An integrated circuit comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phase of the reference signal against phase of the feedback signal, and provide a detector output comprised of a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal; and

a loop filter (LF) operative to receive and filter the detector output and provide an LF output, wherein the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values from the phase-frequency detector.

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10. (Original) The integrated circuit of claim 9, further comprising:
an oscillator operative to receive the LF output and provide an oscillator signal having a phase determined by the LF output; and
a divider operative to receive the oscillator signal, divide the oscillator signal in frequency by a factor of N, where N is one or greater, and provide the feedback signal.

11. (Original) The integrated circuit of claim 9, wherein the loop filter is operative to increase the loop bandwidth if a large phase error between the reference and feedback signals is detected.

12. (Original) The integrated circuit of claim 11, wherein the large phase error is detected if a particular number of consecutive phase error values with same polarity are received in the detector output.

13. (Original) The integrated circuit of claim 9, wherein the loop filter is operative to decrease the loop bandwidth if a small average phase error is detected.

14. (Currently Amended) The integrated circuit of claim 13, An integrated circuit comprising:
a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phase of the reference signal against phase of the feedback signal, and provide a detector output comprised of a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal; and
a loop filter (LF) operative to receive and filter the detector output and provide an LF output, wherein the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values and to decrease the loop bandwidth if a small average phase error is detected, and wherein the small average phase error is detected if, for a designated time window, the number of phase error values with a first polarity, indicating the phase of the reference signal being early, is equal to the number of phase error values with a second polarity, indicating the phase of the feedback signal being early.

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15. (Currently Amended) A device comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phase of the reference signal against phase of the feedback signal, and provide a detector output comprised of a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal; and

a loop filter (LF) operative to receive and filter the detector output and provide an LF output, wherein the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values from the phase-frequency detector.

16. (Currently Amended) An apparatus comprising:

means for comparing phases of a reference signal and a feedback signal to determine a phase error between the reference and feedback signals;

means for providing a detector output comprised of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal;

means for filtering the detector output to obtain a loop filter (LF) output; and

means for adjusting loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values from the means for comparing phases.

Claims 17-29 (withdrawn).

30. (Original) An integrated circuit comprising:

a loop filter (LF) operative to receive and filter an LF input with first and second gains and provide an LF output; and

a control unit operative to receive a detector output from a phase-frequency detector (PFD) indicating whether phase of a reference signal is early or late with respect to phase of a feedback signal, perform phase error analysis on the detector output, and adjust the first and second gains based on results of the phase error analysis, wherein the first and second gains determine loop bandwidth and damping of a digital phase locked loop (PLL) that includes the loop filter and the phase-frequency detector.

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31. (Original) The integrated circuit of claim 30, wherein the detector output comprises a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal.

32. (Original) The integrated circuit of claim 31, wherein the control unit is operative to increase the first gain, the second gain, or both the first and second gains, if a large phase error is detected.

33. (Original) The integrated circuit of claim 32, wherein the control unit is operative to detect for the large phase error by counting number of consecutive phase error values with same polarity and comparing the number of consecutive same polarity phase error values against a predetermined count value.

34. (Original) The integrated circuit of claim 31, wherein the control unit is operative decrease the first gain, the second gain, or both the first and second gains if a small average phase error is detected.

35. (Original) The integrated circuit of claim 34, wherein the control unit is operative to detect for the small average phase error by counting the number of phase error values with a first polarity and the number of phase error values with a second polarity within a designated time window, and wherein the small average phase error is declared if the number of phase error values with the first polarity is equal to the number of phase error values with the second polarity.

36. (Original) An apparatus comprising:
means for receiving a detector output from a phase-frequency detector (PFD) indicating whether phase of a reference signal is early or late with respect to phase of a feedback signal;
means for detecting for a large phase error in the detector output;
means for detecting for a small average phase error in the detector output;

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means for increasing loop bandwidth of a phase locked loop (PLL) if the large phase error is detected; and

means for decreasing the loop bandwidth if the small average phase error is detected.

37. (Original) A method of adjusting loop bandwidth of a digital phase-locked loop (PLL), comprising:

receiving a detector output from a phase-frequency detector (PFD) indicating whether phase of a reference signal is early or late with respect to phase of a feedback signal;

detecting for a large phase error in the detector output;

detecting for a small average phase error in the detector output;

increasing the loop bandwidth if the large phase error is detected; and

decreasing the loop bandwidth if the small average phase error is detected.

Claims 38-44 (withdrawn).

45. (New) The integrated circuit of claim 1, wherein the phase error is a first value if the phase of the reference signal is early with respect to the phase of the feedback signal and is a second value if the phase of the reference signal is late with respect to the phase of the feedback signal.

46. (New) The integrated circuit of claim 45, wherein the phase error is a third value if the phase-frequency detector is unable to discern whether the reference signal is early or late with respect to the feedback signal.

47. (New) The integrated circuit of claim 1, wherein the detector gain is a power of two.

48. (New) The integrated circuit of claim 1, wherein the detector gain is a small value during tracking and is a larger value during acquisition.

49. (New) The device of claim 7, wherein the detector gain is adjusted in an acquisition mode and maintained in a tracking mode.

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50. (New) The device of claim 7, wherein the detector gain is a small value during tracking and is a larger value during acquisition.

51. (New) The apparatus of claim 8, wherein the detector gain is adjusted in an acquisition mode and maintained in a tracking mode.

52. (New) The apparatus of claim 8, wherein the detector gain is a small value during tracking and is a larger value during acquisition.

53. (New) The integrated circuit of claim 30, wherein the first and second gains are powers of two.

54. (New) The integrated circuit of claim 30, wherein the control unit is operative to scale the first and second gains upward by first and second scaling factors, respectively, and to scale the first and second gains downward by third and fourth scaling factors, respectively.

55. (New) The integrated circuit of claim 54, wherein the first and second scaling factors are larger than the third and fourth scaling factors, respectively.